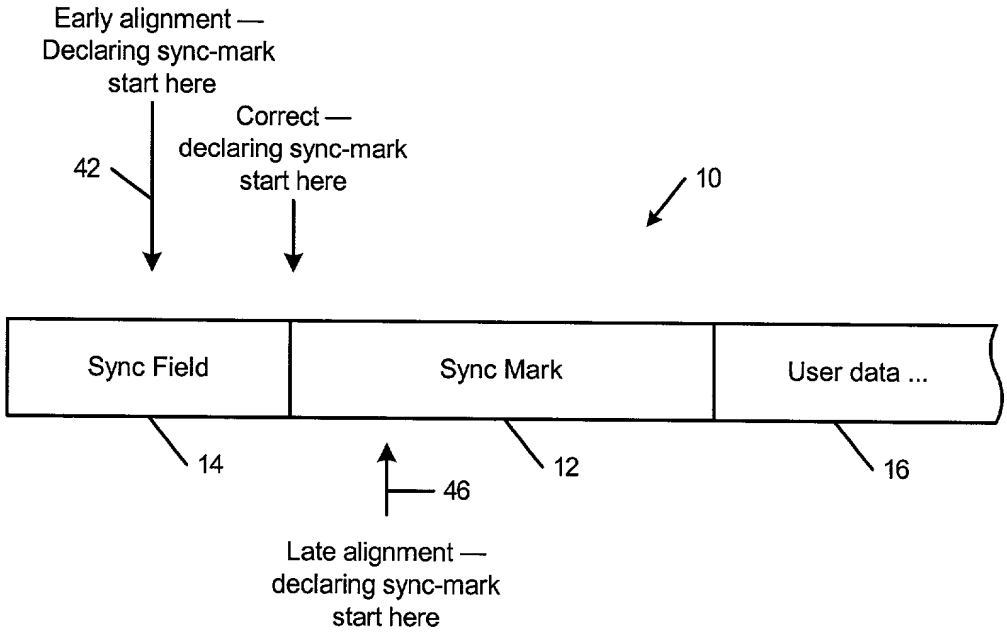



FIG. 1

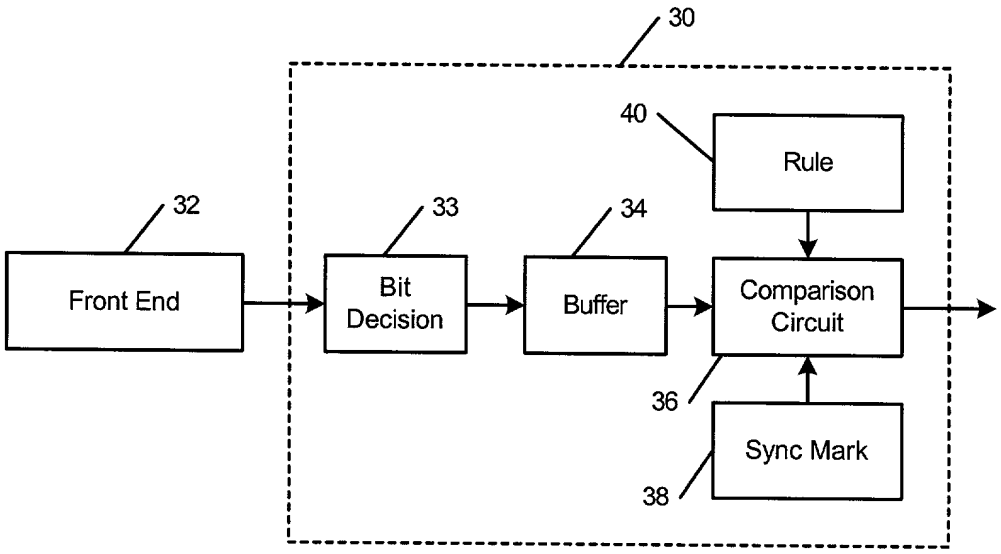
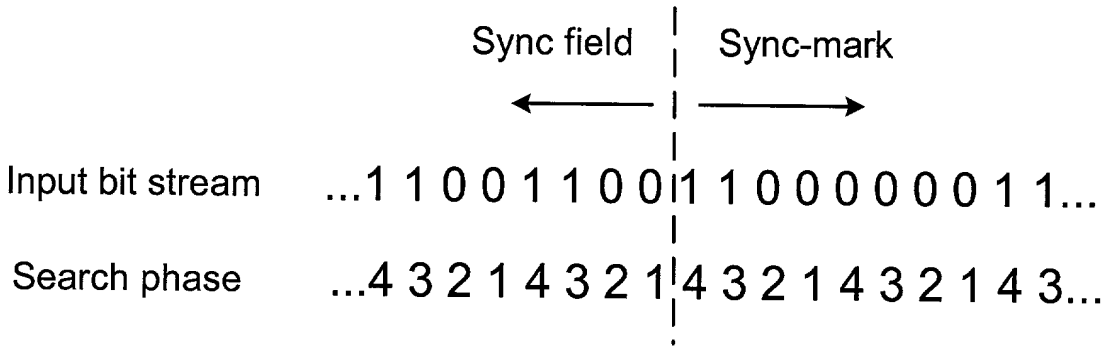



FIG. 2
Prior Art

## FIG. 3

| | |
|---|---|
| Input | 1100110011000000 11 |
| Error-event | 0000-0000000000000 |
| Output | 1100010011000000 11 |

## FIG. 4




## FIG. 5

| NRZ Domain | INRZI Domain |
|---|---|
| +-+ | xx0xx |
| + | x0x |
| +- | xxxx |
| +00+ | x0xx0x |
| +000+ | x0x0x0x |
| +0+ | x000x |

Most Likely Error-Events

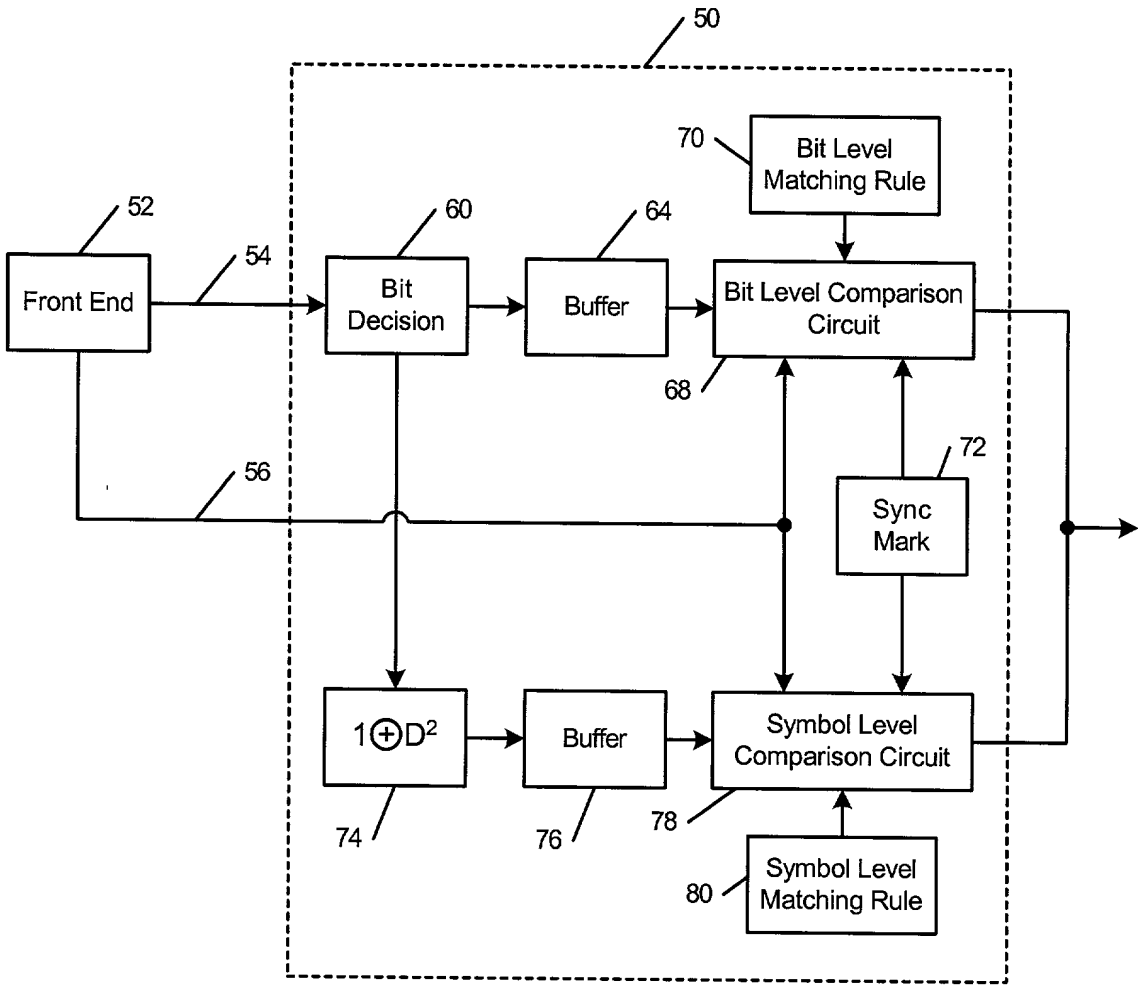

50
70
Bit Level Matching Rule
52
60
64
54
Front End
Bit Decision
Buffer
Bit Level Comparison Circuit
68
72
56
Sync Mark
1⊕D²
Buffer
Symbol Level Comparison Circuit
74
76
78
80
Symbol Level Matching Rule

FIG. 6A

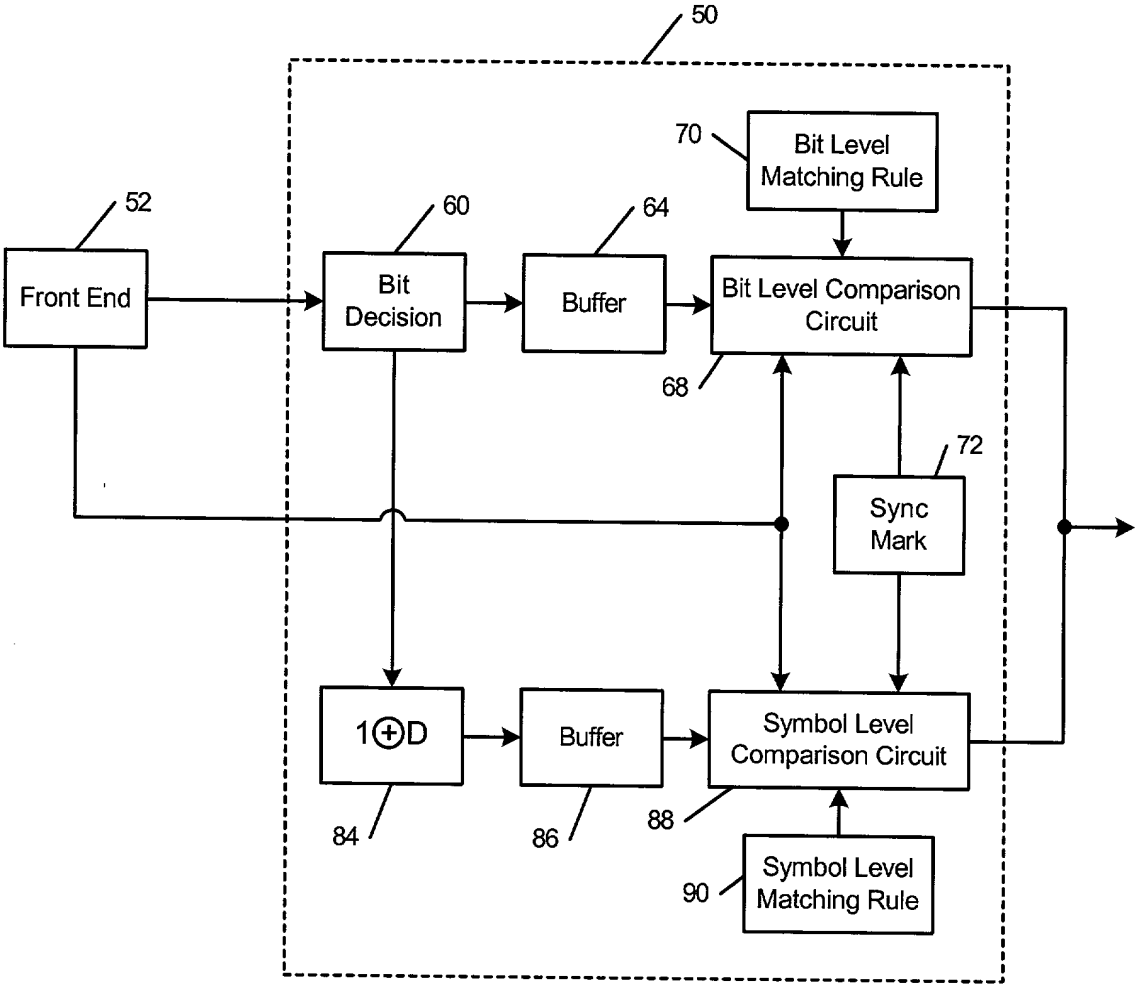



FIG. 6B

| | |
|---|---|
| Sync-mark | bbbbb \| bbbbb \| bbbbb \| bbbbb \| bbbbb \| bbbbb \| bbbbbb |
| NRZ Error-Event | + 00+ |
| INRZI Error-Event | x 0xx0x |

FIG. 7

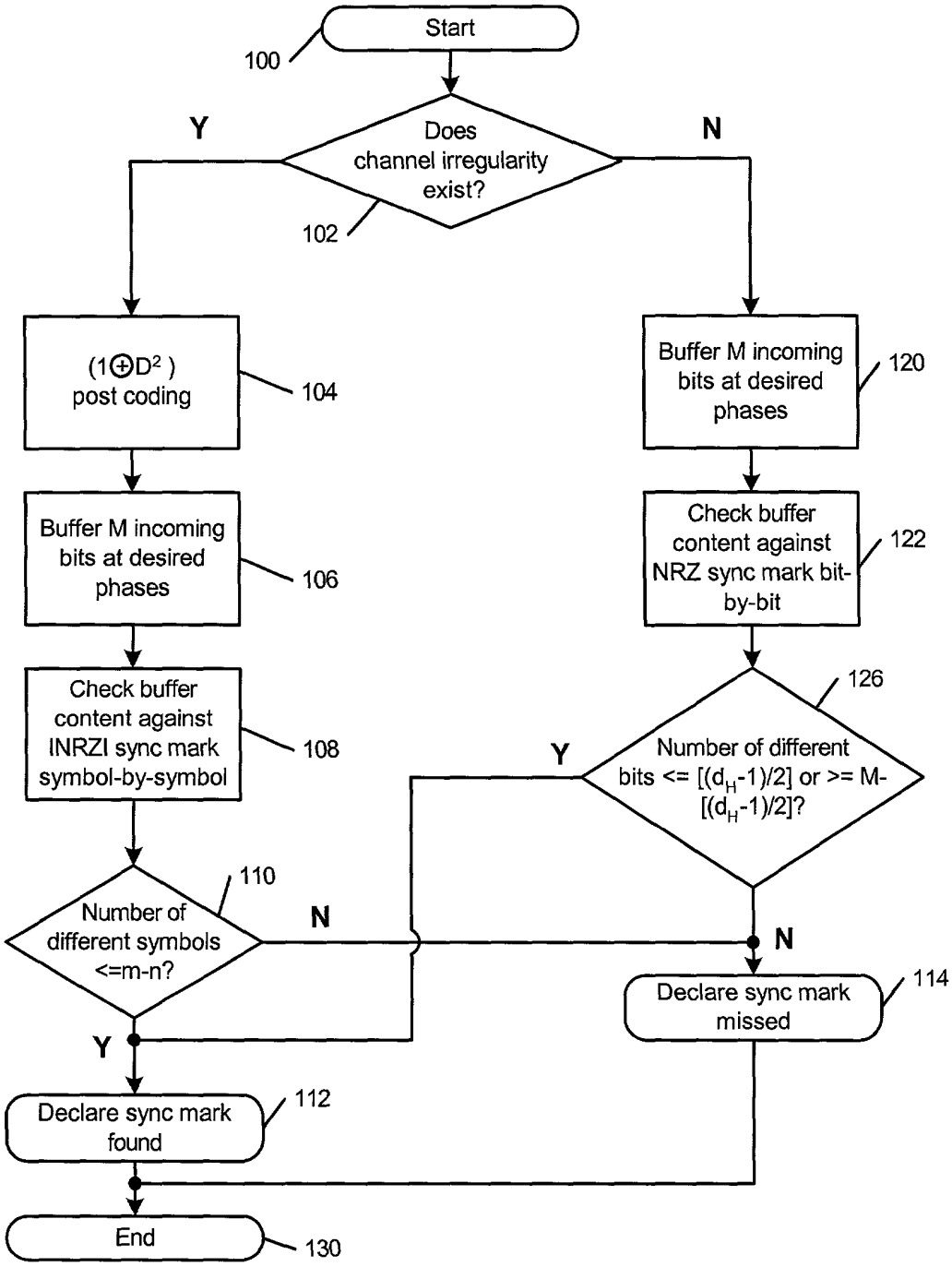

Start
100
Does channel irregularity exist?
102
Y
N
(1⊕D²) post coding
104
Buffer M incoming bits at desired phases
106
Check buffer content against INRZI sync mark symbol-by-symbol
108
Number of different symbols <=m-n?
110
Y
N
Declare sync mark found
112
Buffer M incoming bits at desired phases
120
Check buffer content against NRZ sync mark bit-by-bit
122
Number of different bits <= [(d_H-1)/2] or >= M-[(d_H-1)/2]?
126
Y
N
Declare sync mark missed
114
End
130

FIG. 8

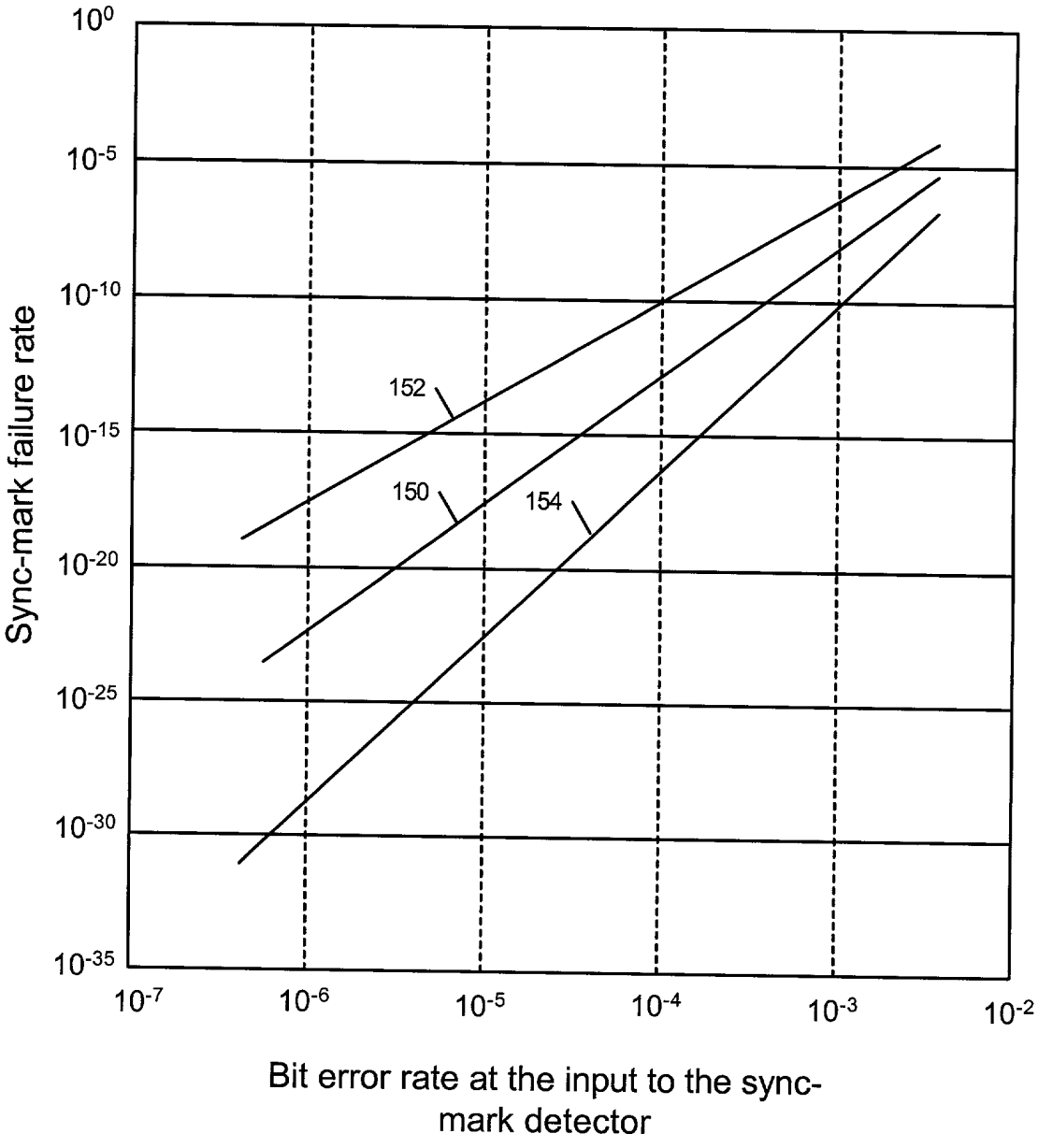

$10^{0}$
$10^{-5}$
$10^{-10}$
$10^{-15}$
$10^{-20}$
$10^{-25}$
$10^{-30}$
$10^{-35}$
Sync-mark failure rate
152
150
154
$10^{-7}$
$10^{-6}$
$10^{-5}$
$10^{-4}$
$10^{-3}$
$10^{-2}$
Bit error rate at the input to the sync-mark detector

**FIG. 9**